In re Patent Application of:
WRIGHT ET AL
Serial No. **10/040,153**
Filed: **JANUARY 2, 2002**

REMARKS

Claims 1-16 are pending.

Of the originally presented claims, claims 7 and 12 have been amended to eliminate the objection raised in paragraph 1 on page 2 of the Office Action. In addition, paragraphs [06] of the specification and [26] have been amended to eliminate obvious typographical errors.

Reconsideration of this application in light of the foregoing amendments and following remarks is respectfully requested.

The objection to line 2 of step (c) of each of claims 7 and 12 is well taken. As correctly inferred in the Office Action, the output signal to which reference is made is that produced in step (b). Step (c) of each of claims 7 and 12 has been amended to properly refer back to (b), where antecedent basis for the output signal is set forth. Withdrawal of the objection to claims 7 and 12 is, accordingly, earnestly solicited.

The rejection of claims 1-16 under the provisions of 35 U.S.C. § 102, as allegedly being anticipated by the patent application publication to Rakib et al, is respectfully traversed.

Before addressing the shortcomings of the reference to Rakib et al, the present invention will be briefly reviewed, in order that differences between the cited prior art and the present invention, particularly as delineated in claims 1-16, may be more readily appreciated.

As is described in the initial portion of the present specification, in order to achieve successful reception and parsing of respective cells of a serial data stream, such as an ATM-based serialized data stream, it is imperative that the start of respective octets or bytes of which the ATM cells are comprised be delineated. Unless such byte boundaries can be found, recovery of the data stream will not be successful.

The present invention is directed to a mechanism and method for locating boundaries of the respective bytes of the incoming data stream, so that respective cells of the data stream may be delineated. For this purpose, the present invention employs a counter which counts respective clock signals associated with the incoming serial data stream. Coupled with the counter is a synchronization signal derivation unit that generates an output signal, which is potentially aligned with the boundary of a byte of the incoming serial data stream. This output (frame sync) signal FS is produced in response to the counter reaching a prescribed count value. When this happens, the receiver's cell delineation mechanism determines whether cell delineation within a prescribed cell delineation acquisition window (some number of frame sync signals FS) has been achieved. If cell delineation is not achieved within this window, the time at which the output signal is produced relative to the counting operation of the counter is iteratively shifted, until the output signal eventually becomes aligned with the boundary of a byte in the incoming serial data stream.

Two implementations of the invention are disclosed and claimed. A first embodiment, described in paragraphs [20]-[26] of the specification, employs a logic circuit 60, which monitors the output of the counter 30, and a control processor 40, which is coupled to the cell delineation mechanism. If byte alignment is not achieved after some number of FS signals, the control

processor 40 causes the counter 30 to be preloaded with a different value by way of the multiplexer 50, so as to effectively shift the frame sync signal FS by one bit time, causing the cell delineation mechanism to use a different bit, than that employed previously, as a new start-of-octet location.

In accordance with the second embodiment, shown in Figure 4 and described in paragraphs [27]-[34] of the specification, a shift register 140, which is coupled to monitor the output of the counter 130, is coupled to a multiplexer 150 through which the output signal FS is produced. If the receiver's cell delineation mechanism does not achieve cell delineation within a prescribed cell delineation acquisition window, the control processor 40 will change the control input to the multiplexer 150 for the next frame sync count period, so as to step to a new stage of the shift register, and thereby effectively shift the location used for byte delineation.

Each of independent claims 1, 7 and 12, upon which respective claims 2-6, 8-11 and 13-16, respectively, depend, recites the fact that the output signal (corresponding to the frame sync signal FS) is produced in potential alignment with the boundary of a byte of the incoming serial data stream, in response to the contents of the counter reaching a prescribed value. In addition, the independent claims recite that the time at which the output signal is produced, relative to the counting operation of the counter, is iteratively shifted, as necessary, until the output signal is aligned with the boundary of a byte of the incoming serial data stream.

Applicants have carefully reviewed the cited reference to Rakib et al 2001/0046266, but have been unable to find any disclosure or suggestion of the problem to which the invention is

directed, much less the solution thereto as specifically set forth in claims 1-16.

Contrary to what applicants respectfully submit has been mischaracterized in the statement of the rejection in paragraph 4 on pages 2 and 3 of the outstanding Office Action, Rakib et al do not have any cell delineation mechanism for locating the boundaries of respective bytes of the incoming serial data stream, much less one which employs the counter shifting mechanism, the operation of which is iteratively shifted until byte alignment occurs, as claimed in claims 1-16.

Paragraphs [0009], [0010] of Rakib et al, to which reference is made in the initial portion of paragraph 4 on page 2 of the Office Action, discuss the need for receiver clock synchronization in general, but do not describe what has been erroneously attributed to Rakib et al in the cited paragraph.

Paragraph [0021] of column 3 of the Rakib et al publication also does not contain the description of anything which is used to provide byte alignment and thereby delineate respective cells in the data stream.

Paragraph [0263] bridging pages 22 and 23 of the cited Rakib et al publication, refers to Figure 14, and describes that a first 9-bit byte is stored in the lowest row of the lowest three blocks in the left hand column of a pictorially represented memory diagram, previously described in paragraphs [0261]-[0262].

Paragraphs [0322] and [0540] of the Rakib et al publication described that a CPU is informed of which time slots are currently being received from an orthogonal multiplexer or other circuitry not shown, which is used to reassemble ATM packets

using the 9th bit cell delimiter codes in the manor described in a document not included in the Office Action.

The portions of a cited reference do not describe a mechanism for achieving byte alignment, namely, locating boundaries of respective bytes of an incoming serial data stream.

What in fact is disclosed by the cited Rakib et al publication is discussed in paragraphs [0256]-[0260] on page 22 of the document, which references Figure 9. The problem addressed by Rakib et al is the need to provide some mechanism that implements a variable delay to maintain frame synchronization of receivers at a plurality of remote units (RUs) with a transmitter located at a central unit (CU). In the block diagram of Rakib et al's framer circuit shown in Figure 9, this is achieved by imparting a delay T_d, as necessary, to the receive clock, by selectively reading out data that has been loaded into a memory at a variable read-out time, to achieve the desired delay T_d. As described in the last four lines of paragraph [0259] of Rakib et al this delay maybe some fraction of the number of bit clocks making up an entire 9-bit byte. This is because the delay needed to maintain frame synchronization may not work out to be an integer number of byte clocks.

This statement by Rakib et al makes it readily apparent that Rakib et al are not concerned with achieving byte alignment, but are rather concerned with maintaining frame synchronization with a central unit transmitter. That frame synchronization is maintained by controllably reading data out of the memory 300 at the same rate at which it was stored, but starting at some programmable (variable) time after the data is stored, as described in lines 1-5 of paragraph [0258] of the Rakib et al publication.

Moreover, the byte counter 370 described in paragraph [0256] of Rakib et al, to which reference is made in the statement of the rejection in item 4 of pages 2 and 3 of the outstanding Office Action, is simply that, a byte counter. There is no disclosure of a synchronization signal derivation unit as particularly delineated in claim 1, nor the methodology of steps (c) of claims 7 and 12, in the disclosure of the publication to Rakib et al relative to the operation of the byte counter. Paragraphs [0343] and [0429]-[0430] of Rakib et al contain no disclosure or suggestion of being concerned with byte alignment and iteratively shifting, as necessary, the time of which the output signal is produced relative to the counting operation of the counter until the output signal is aligned with the boundary of a byte of the incoming serial data stream. The delay implementation mechanism of Figure 9 of Rakib et al is implemented by programmably adjusting the read out time of the contents of memory 300 relative to the write in time, so as to implement a variable delay T_d to maintain frame synchronization. Byte alignment is not addressed.

As the publication to Rakib et al does not disclose or suggest the basic mechanism and methodology set forth in claims 1, 7 and 12, it certainly does not disclose the details of the implementation of that mechanism and methodology, as set forth in dependent claims 2-6, 8-11 and 13-16.

Applicants do not deny the fact that the system of Rakib et al employs signal processing components, such as counters, logic circuits, a control processor, shift registers, and the like. However, the system of Rakib et al in which such components are employed, is entirely different from that of Applicants' claimed invention.

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In the absence of a citation of prior art, which addresses the problem with which the present invention is concerned, and the solution thereof, as delineated in claims 1-16, withdrawal of the rejection set forth in the outstanding Office Action and a notice of allowability of claims 1-16 are respectfully requested.

Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 01-0484 and please credit any excess fees to such deposit account.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number **571-273-8300** to MAIL STOP AMENDMENT, COMMISSIONER FOR PATENTS, this 1 day of March 2006.